UNIVERSITY OF CALIFORNIA IRVINE

EECS 221: Languages and Compilers for Hardware Accelerators

(Winter 2022)

Instructor

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- Office Hours: Tuesdays 9:30-10:30 am or by appointment

Lecture Time and Location

- Time: Tuesdays/Thursdays 8:00-9:20 am
- Location: SSTR 101 or online (please check Canvas for the latest announcements)

Course Description

Hardware accelerators have been seen in many new application domains and they greatly improve the performance and energy efficiency of computing systems. However, programming and optimizing hardware accelerators are challenging. Programming languages and optimizing compilers are the key to improve the programming efficiency unleash the full power of hardware accelerators. This course will cover the essential concepts and techniques in programming languages and compilers designed for hardware accelerators, including different approaches of designing languages for accelerators, the considerations of language features, compiler optimization techniques for hardware accelerators, etc. We will discuss these concepts and techniques using state-of-the-art research works in the field as examples.

Prerequisites

Basic understanding of digital circuits and computer architecture.

Grading Policy

- Homework: 30%
- Midterm: 30%
- Project: 40%

Tentative Schedule

- Week 1: Course Introduction
- Week 2: Hardware Accelerators
- Week 3: Language and Compiler Basics
- Week 4: Reconfigurable Accelerators
- Week 5: High-Level Synthesis
- Week 6: *Midterm*
- Week 7: Compiler Optimizations for Accelerators
- Week 8: Machine Learning Compilers
- Week 9: Emerging Architectures and Compilers
- Week 10: *Project Presentations*

NOTE: Please check Canvas for the latest announcements